AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A ~~current compensation circuit for use with a current mirror circuit, the current mirror circuit having a current path defined by a first programmable current mirror stage driving a first fanout current mirror stage, the first programmable current mirror stage having at least one transistor with a channel length exhibiting a first channel length modulation factor λ1, the first fanout current mirror stage coupled to a supply voltage source, the current compensation~~ circuit comprising:

a supply voltage current mirror configured to be coupled to ~~the~~ a supply voltage source, and comprising ~~having~~ a current output configured to be coupled to a node ~~the current path~~; the node coupling a fanout current mirror and a first programmable current mirror, the first programmable mirror having a first channel length modulation factor λ1; and

a second programmable current mirror coupled to ~~in series with~~ the supply voltage current mirror and ~~having at least one~~ comprising a second transistor ~~with~~ having ~~a channel length exhibiting~~ a second channel length modulation factor λ2, ~~wherein~~ the second channel length modulation factor λ2 ~~is~~ being larger than the first channel length modulation factor λ1, ~~the first programmable current mirror and~~ the second programmable current mirror being configured

~~cooperating~~ to maintain, with the first programmable current mirror, a bias current through the fanout current mirror substantially independent of voltage changes in the supply voltage source.

2. (Currently Amended) ~~A current compensation~~ The circuit ~~according to~~ of claim 1 wherein ~~each of~~ the first programmable current mirror ~~stages~~ comprises[[:]] a parallel array of programmable transistors for defining a predetermined range of current.

3. (Currently Amended) ~~A current compensation~~ The circuit ~~according to~~ of claim 1 wherein the ~~current compensation~~ circuit is formed on a single integrated circuit device.

4. (Currently Amended) ~~A current compensation~~ The circuit ~~according to~~ of claim 3 wherein the ~~current compensation~~ circuit is formed ~~in CMOS~~ using complementary metal-oxide-semiconductor technology.

5. (Currently Amended) A ~~current compensation circuit for use with a current mirror circuit, the current mirror circuit having a current path defined by a first programmable current mirror stage driving a first fanout current mirror stage, the first programmable current mirror stage having at least one transistor with a channel length exhibiting a first channel length modulation factor λ1, the first fanout current mirror stage coupled to a supply voltage source, the current compensation~~ circuit comprising:

a means for detecting changes in the ~~supply~~ voltage from ~~the~~ a supply voltage source, the means for detecting changes comprising a ~~including~~ means for generating a compensation signal representative of voltage changes in the supply voltage source; and

a means for generating a compensation current for application to ~~the~~ a current mirror in response to the compensation signal.

6. (Currently Amended) ~~A current compensation~~ The circuit ~~according to~~ of claim 5 wherein the means for detecting voltage changes in the supply voltage source comprises:

a supply voltage current mirror configured to be coupled to the supply voltage source, and ~~having~~ comprising a current output configured to be coupled to a node ~~the current path~~, the node coupling a fanout current mirror and a first programmable current mirror, the first programmable mirror having a first channel length modulation factor $\lambda 1$, the current mirror coupled to the supply voltage source; and

a second programmable current mirror coupled to ~~in series with~~ the supply voltage current mirror .

7. (Currently Amended) ~~A current compensation~~ The circuit ~~according to~~ of claim 6 wherein[[:]]

the second programmable current mirror comprises a second ~~includes at least one~~ transistor having ~~with a channel length exhibiting~~ a channel length modulation factor $\lambda 2$, ~~such~~

~~that~~ the second channel length modulation factor λ2 ~~is~~ being larger than the first channel length modulation factor λ1; and

the means for generating a compensation current comprises the ~~first and~~ second programmable current mirror ~~mirrors~~ cooperating to maintain a bias current through the first fanout current mirror stage substantially independent of changes in the supply voltage source.

8. (Currently Amended) A method for compensating for supply-voltage-induced changes to a desired current through a fanout current mirror, the method comprising ~~including the steps~~:

detecting changes in the ~~supply~~ voltage from a supply voltage source;

generating a compensation current to a current path node, the compensation current representative of the voltage changes in the supply voltage source, the compensation current based on the channel length modulation factor λ2 of a second programmable current source; and

sinking current from the current path node with a first programmable current source having a first channel length modulation factor λ1, λ1 being less than ~~that of~~ λ2, wherein the level of current sunk corresponds to the difference between the compensation current and the desired current through the fanout current mirror.

Claims 9 to 12 (Cancelled)

Claim 13 (New) A circuit, comprising:

a current mirror circuit, the current mirror circuit comprising:

a first programmable current mirror and a fanout current mirror coupled to the first programmable current mirror by a node, the first programmable current mirror comprising a first transistor having a first channel length modulation factor $\lambda 1$, the fanout current mirror coupled to a supply voltage source, and

a current compensation circuit; the current compensation circuit comprising:

a supply voltage current mirror coupled to the supply voltage source and comprising a current output coupled to the node; and

a second programmable current mirror coupled to the supply voltage current mirror comprising a second transistor with a second channel length modulation factor $\lambda 2$, the second channel length modulation factor $\lambda 2$ being larger than the first channel length modulation factor $\lambda 1$, the first programmable current mirror and the second programmable current mirror cooperating to maintain a bias current through the fanout current mirror substantially independent of voltage changes in the supply voltage source.

Claim 14 (New) The circuit of claim 13 wherein the first programmable current mirror comprises a parallel array of programmable transistors for defining a predetermined range of current.

Claim 15 (New) The circuit of claim 13 wherein the second programmable current mirror comprises a parallel array of programmable transistors for defining a predetermined range of current.

Claim 16 (New) The circuit of claim 13 wherein the circuit is formed on a single integrated circuit device.

Claim 17 (New) The circuit according to claim 13 wherein the circuit is formed using a complementary metal-oxide-semiconductor.